TOSHIBA INTEGRATED CIRCUIT
TECHNICAL DATA

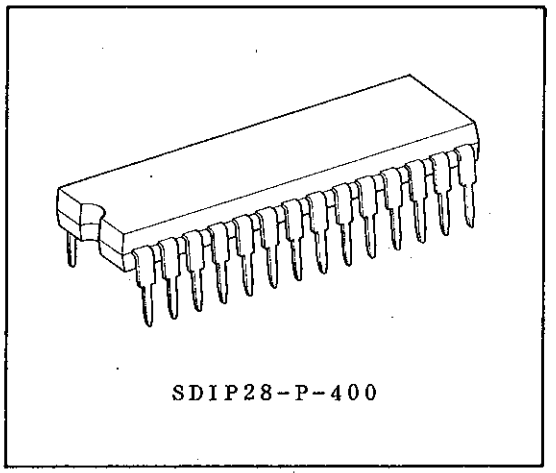
TC9231N

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

MODULATION AND TRANSMISSION IC FOR DIGITAL AUDIO INTERFACE

TC9231N is a modulation and transmission IC according to the standard of Electronic Industries Association of Japan for digital audio interface.

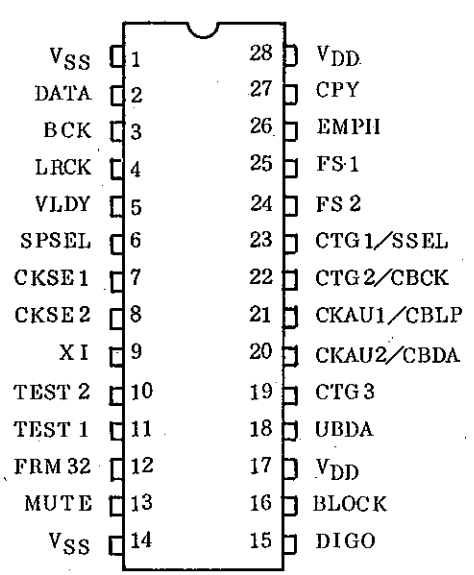
- EIAJ Digital Audio Interface format output by connecting with proccessor LSI for digital audio (PCM decoder for CD, DAT, BS tuner and others).
- Channel status data (C bit) transmission by setting terminals (CTG1, CTG2 ...) or by inputting data serially from Microprocessor. (Serial 32 bit from the head of channel status data or all 192 bit channel status data)
- User data transmission is possible.
- High speed, Low power dissipation, CMOS silicon gate structure.
- Outline is 28 pin shrink DIP typ.



SDIP28-P-400

Weight :2.2g (Typ.)

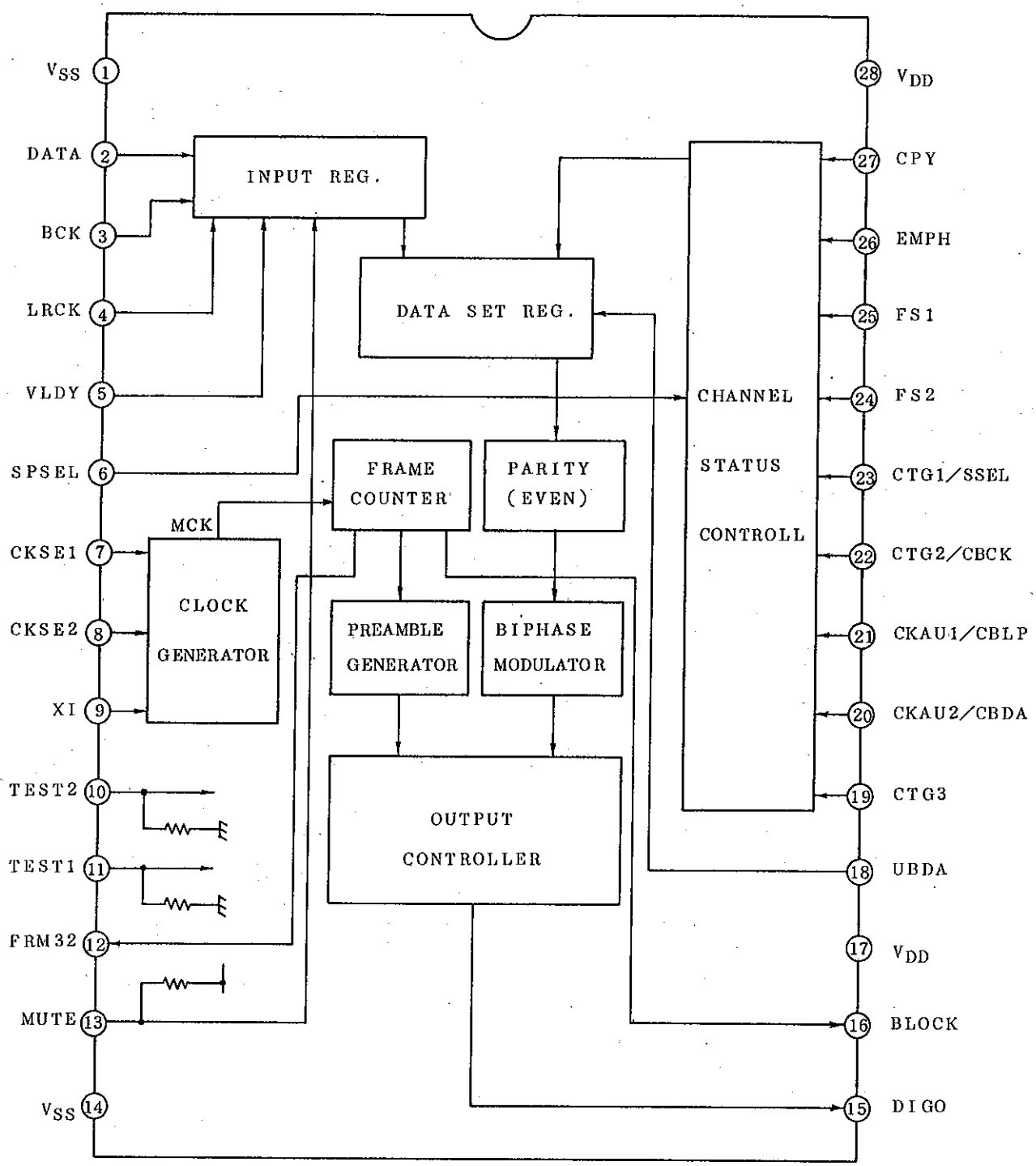
PIN CONNECTION (TOP VIEW)



MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	-0.3~7.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Power Dissipation	P_D	800	mW
Storage Temperature	T_{stg}	-40~125	°C
Operating Temperature	T_{opr}	-20~70	°C

BLOCK DIAGRAM



FUNCTION OF EACH PIN

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
1	V_{SS}	-	Ground terminal.	
2	DATA	I	Data input terminal.	
3	BCK	I	Bit clock input terminal.	
4	LRCK	I	Channel clock input terminal.	
5	VLDY	I	Validity-flag input terminal. "H"-Compensated data "L"-Uncompensated data	
6	SPSEL	I	Input mode setting terminal for channel status bit.	
7	CKSE1	I	XI clock deviding ratio setting terminal.	
8	CKSE2	I		
9	XI	I	Input terminal for function master clock.	
10	TEST2	I	Test terminal. Normally, "L" or open.	With pull-down resistor
11	TEST1	I	Test terminal. Normally, "L" or open.	With pull-down resistor
12	FRM32	O	Clock terminal, 1 period = 32 frames.	
13	MUTE	I	Muting terminal. Muting on low level.	With pull-up resistor
14	V_{SS}	-	Ground terminal.	
15	DIGO	O	Data output terminal based on Digital Audio interface format.	
16	BLOCK	O	Output terminal marking the block head.	
17	V_{DD}	-	Power supply voltage terminal.	
18	UBDA	I	User data input terminal.	
19	CTG3	I	Category code setting terminal.	

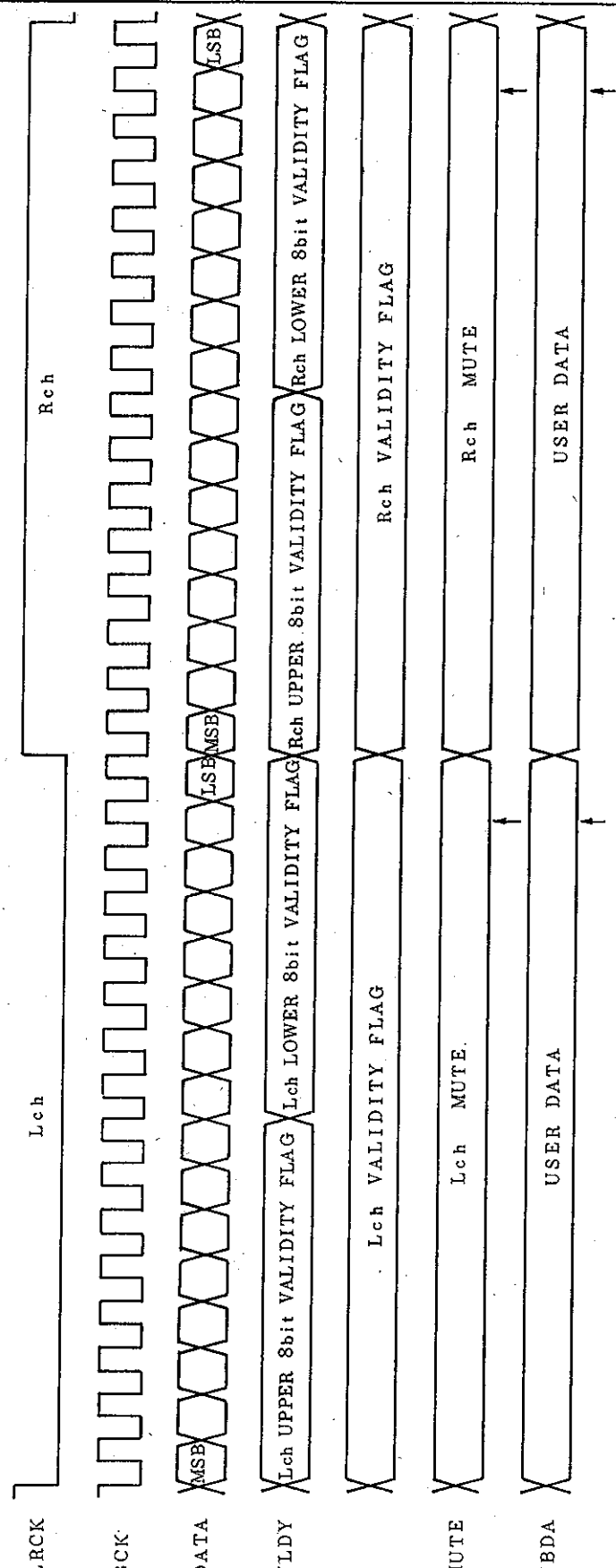
PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
20	CKAU2 /CBDA	I	Clock accuracy setting terminal. (SPSEL="H") Channel status data serial input terminal. (SPSEL="L")	
21	CKAU1 /CBLP	I	Clock accuracy setting terminal. (SPSEL="H") Latch palse input terminal for serial channel status data. (SPSEL="L")	
22	CTG2 /CBCK	I	Category code setting terminal. (SPSEL="H") Bit clcok input terminal for serial channel status data. (SPSEL="L")	
23	CTG1 /SSEL	I	Category code setting terminal. (SPSEL="H") Serial input mode selection terminal for channel status data. (SPSEL="L")	
24	FS2	I	Sampling frequency set terminal for channel status data.	
25	FS1	I	Sampling frequency set terminal for channel status data.	
26	EMPH	I	Emphasis setting terminal for channel status data.	
27	CPY	I	Copy bit setting terminal for channel status data.	
28	V_{DD}	-	Power supply voltage terminal.	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD}=5.0V, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage		V_{DD}	-	Ta=-20~70°C		4.5	5.0	5.5	V
Operating Power Supply Current		I_{DD}	-	f_{XI}=18.432MHz CKSE1="L" CKSE2="L"		-	-	15	mA
Input Voltage	"H" Level	V_{IH}	-	All input terminals.		4.0	-	-	V
	"L" Level	V_{IL}	-			-	-	1.0	
Input Current	"H" Level	I_{IH}	-	V_{IN}=5V	All input terminals except TEST1,TEST2 terminals.	-	-	1.0	μA
	"L" Level	I_{IL}	-	V_{IN}=0V	All input terminals except MUTE terminal.	-1.0	-	-	
Output Current	"H" Level	I_{OH}	-	V_{OH}=4.6V	DIGO	-	-	-4.0	mA
					FRM32, BLOCK	-	-	-1.0	
	"L" Level	I_{OL}	-	V_{OL}=0.4V	DIGO	8.0	-	-	
					FRM32, BLOCK	2.0	-	-	
Pull-up Resistor		R_{UP}	-	MUTE		-	70	-	kΩ
Pull-down Resistor		R_{DOWN}	-	TEST1, TEST2		-	70	-	kΩ

Fig. 1 INPUT TIMING

Case of $f_{BCK}=32f_{LRCK}$



DESCRIPTION OF BLOCK OPERATIONS

1. Digital Audio Data Input Block

DATA : Input digital audio data.
Input digital audio data, 16 bits serially, MSB first and back justify to LRCK or at equal spaces.
Further, input data synchronously with falling of BCK.

BCK : More than 16 bits clocks in a cycle of data bit rate are required per word.

LRCK : Input clocks in a cycle of sampling rate, that become "L" level when digital audio data is in Lch and "H" level when digital audio data is in Rch.

VLDY : Input the validity flag.
Input "H" if data is corrected or interpolated erroneous data and input "L" if data is correct.
If the validity flag is not used, fix this at "L" level.

MUTE : At "L" level, only the digital audio sample word of DIGO (Digital Out) output becomes "0".
Further, the MUTE signal is taken in at the rise of the 14th bit of the clock input to the BCK terminal (as shown in Fig. 1) and at the same time, input data only is made "0".
At "H" level, DIGO is the ordinary output.

2. Clock Generator Block

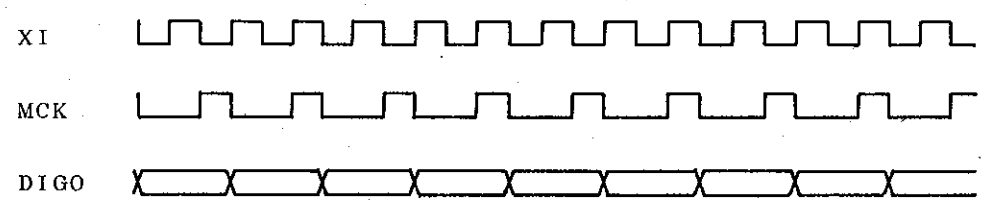
This block generates master clock in LSI by dividing clock inputting to XI.
Set CKSE1 and CKSE2 as shown in the following table according to frequency to be input to XI.

XI	CKSE2	CKSE1
384Fs	L	L
256Fs	L	H
128Fs	H	L
192Fs	H	H

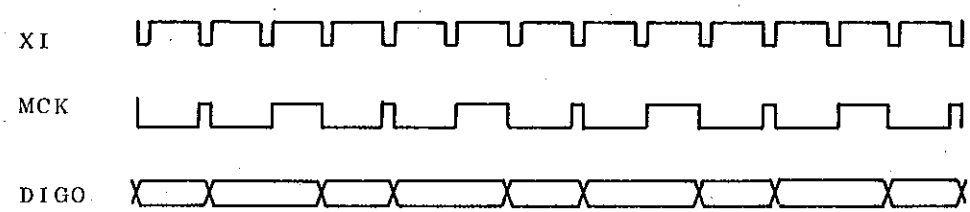
Fs : Sampling frequency

If 192Fs was selected (CKSE2="H", CKSE1="H"), DIGO output may have jitter depending upon duty of clock to be input to XI.

Duty=50%



Duty≠50%



3. TEST1, TEST2 : Test terminal. Normally, use this terminal at "L" level.

4. Output Control Block

DIGO : Digital Out output terminal based on digital audio interface format.

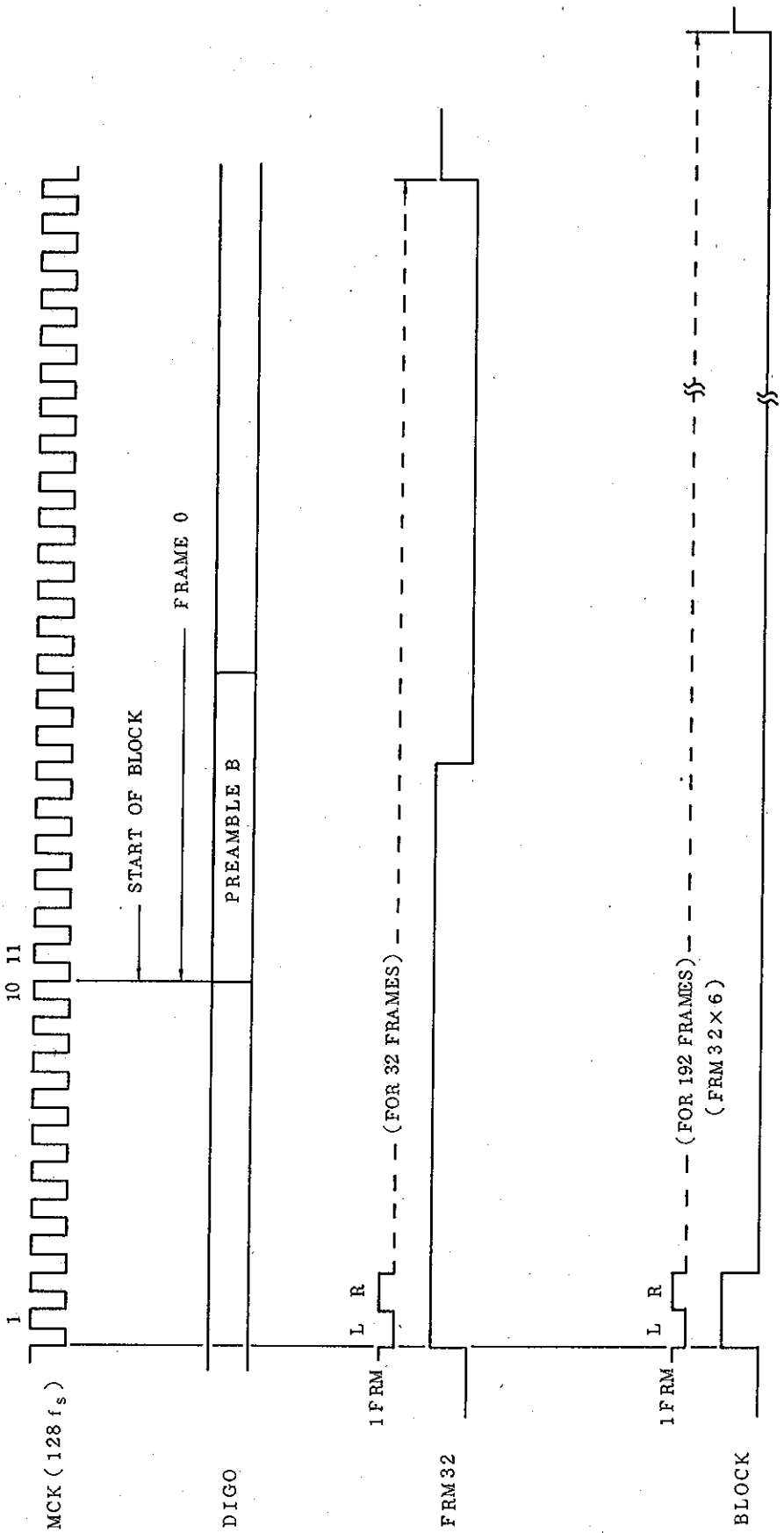


Fig. 2 OUTPUT TIMING

5. Channel Status Control Block

SPSEL : The channel status data (C Bit) input mode setting terminals.
Directly set channel status data at terminals 20~27 when "H" level.
All bits other than set are "0".
Serially input channel status data when "L" level.
At this time, 2 kinds of serial input modes are selectable by CTG1/SSEL.

5.1 DC Setting Mode

DC set each channel status data through the following terminals:

CPY : Disable/enable of digital copy.
"L" Digital copy is disabled.
"H" Digital copy is enabled.

EMPH : Availability of pre-emphasis.
"L" No pre-emphasis is available.
"H" Pre-emphasis of 50/15 μsec is available.

FS1, FS2 : Sampling frequency

FS1	FS2	Sampling Frequency
L	L	44.1kHz
L	H	48kHz
H	H	32kHz
H	L	-

CTG1/SSEL, CTG2/CBCK : Category Code

CTG1/SSEL	CTG2/CBCK	CTG3	Category Code
L	L	L	2ch general format
L	H	L	2ch PCM encoder/decoder
H	L	L	2ch compact disc player
H	H	L	2ch digital audio tape recorder
L	L	H	Satellite broadcasting (DBS)

CKAU1/CBLP, CKAU2/CBDA : Clock Accuracy

CKAU1/CBLP	CKAU2/CBDA	Clock Accuracy
L	L	Level II
L	H	Level III
H	L	Level I
H	H	-

5.2 Serial Input Mode

CTG1/SSEL : 2 kinds of serial input modes are selected.
When "L" level, input 32 bits from the top among channel status data 192 bits and use the initially input data until data is input again.
When "H" level, it is possible to input all 192 bits of channel status data by inputting 32 bits are at a time.

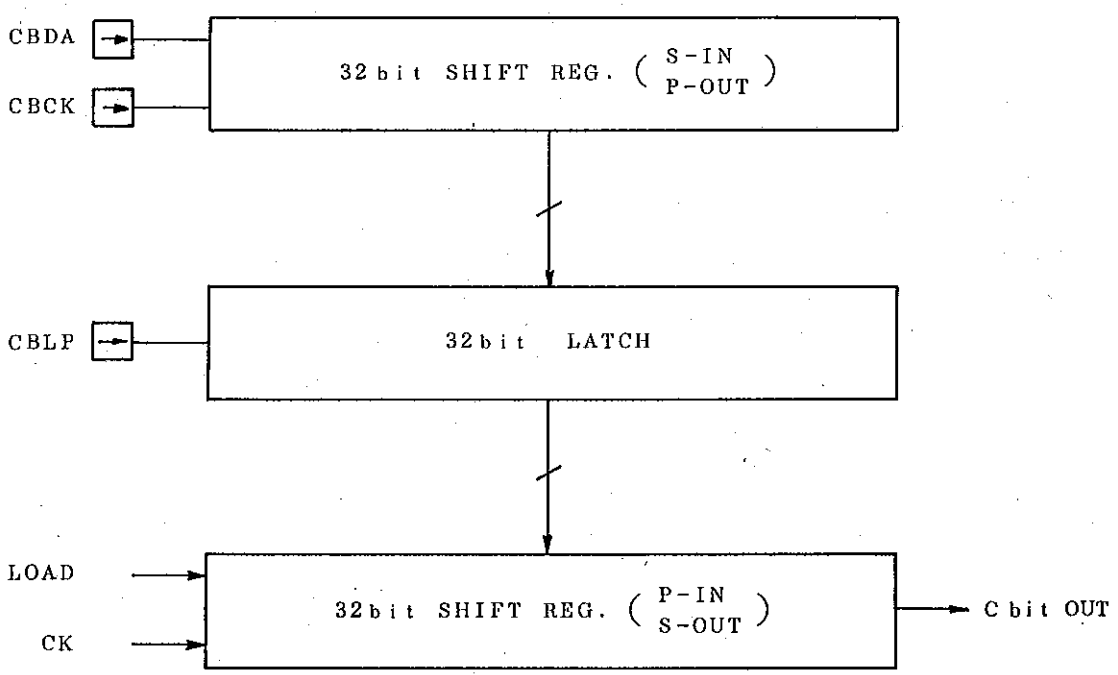
CTG2/CBCK : Input clocks in a cycle of bit rate of inputting channel status data.

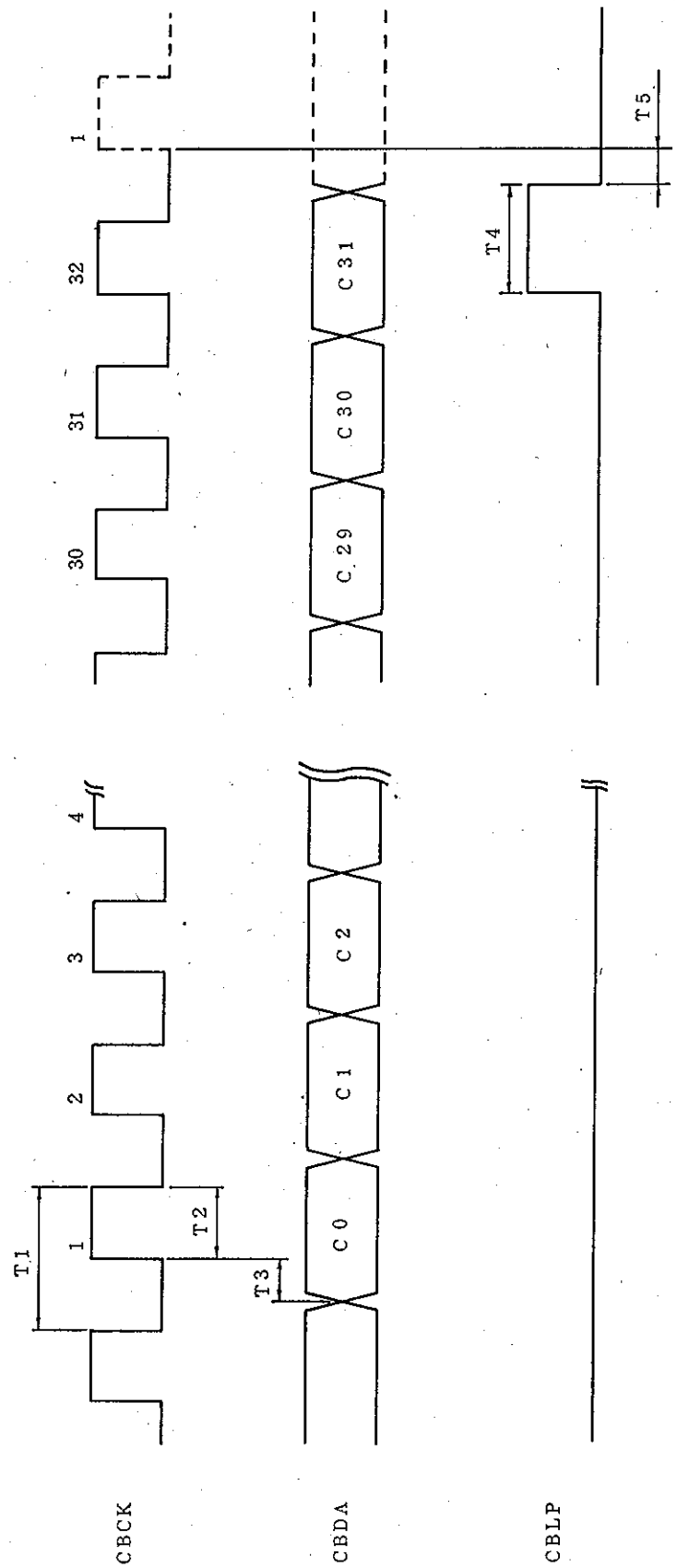
CAKU1/CBLP: Input latch pulse to latch inputting channel status data.

CKAU2/CBDA: Input channel status data.

Input Mode / Terminal	Serial Input Mode (SPSEL=L)	DC Setting Mode (SPSEL=H)	REMARKS
CPY	-	Copy enable/disable	
EMPH	-	Availability of emphasis	
FS1	-	Sampling frequency	
FS2	-	Sampling frequency	
CTG1/SSEL	Serial input mode selection	Category code	
CTG2/CBCK	Bit clock	Category code	
CKAU1/CBLP	Latch pulse	Clock accuracy	
CKAU2/CBDA	Channel status data	Clock accuracy	
CTG3	-	Category code	

Fig. 3 C BIT SERIAL INPUT CIRCUIT BLOCK DIAGRAM





T1 ≧ 10.0 (μs)
T2 ≧ 1.0 (μs)
T3 ≧ 1.0 (μs)
T4 ≧ 1.0 (μs)
T5 ≧ 5.0 (μs)

Fig. 4 C BIT SERIAL INPUT TIMING

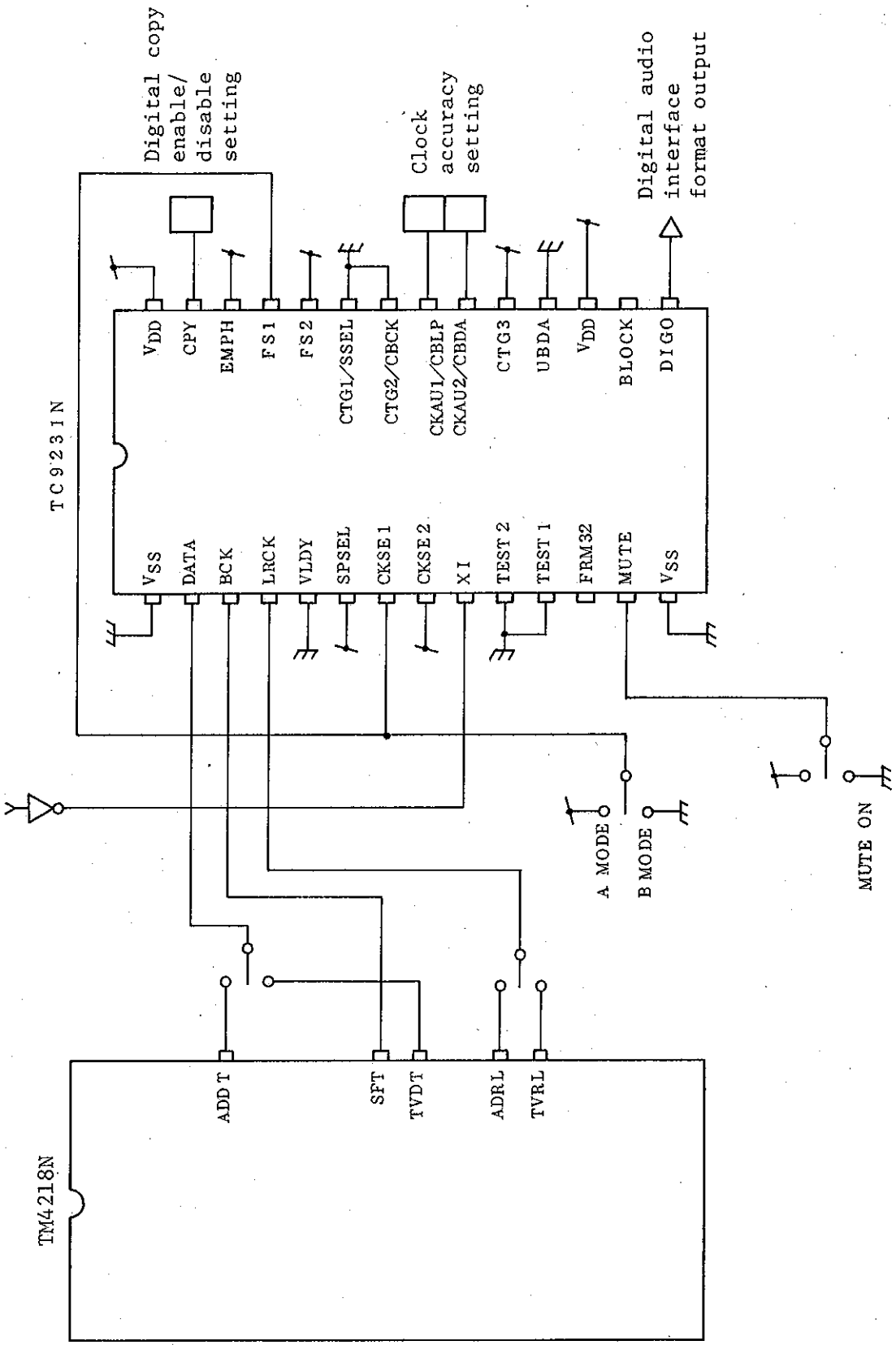
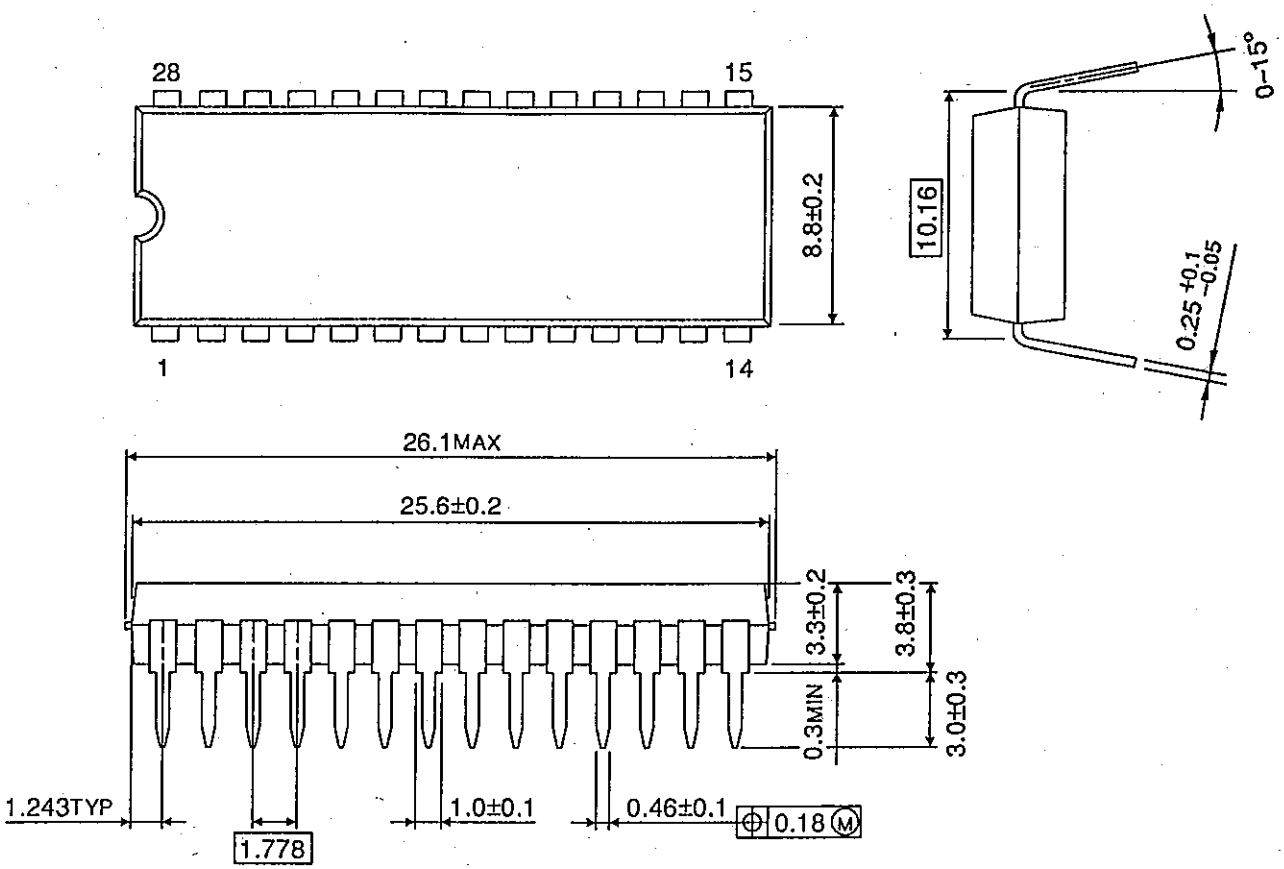


Fig. 5 TC9231N-TM4218N EXAMPLE OF CONNECTION

OUTLINE DRAWING
SDIP28-P-400

Unit in mm



Weight : 2.2g (Typ.)